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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,031	03/31/2004	Hiroki Goko	030712-36	3838
78198	7590	04/14/2010	EXAMINER	
Studebaker & Brackett PC One Fountain Square 11911 Freedom Drive, Suite 750 Reston, VA 20190			MEMULA, SURESH	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,031	GOKO ET AL.	
	Examiner	Art Unit	
	SURESH MEMULA	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 21 January 2010.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-5 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-5 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 31 March 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____.	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION

This office action is a response to the Appeal Brief filed on 01/21/2010. The §102(e) rejections under Weaver are withdrawn. However, in view of the newly considered prior art detailed below, this application is not in condition for allowance. Claims 1-5 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1 and 3 are rejected under 35 U.S.C. 102(b)** as being anticipated by US Patent No. 6,289,498 to Dupenloup (Hereinafter: Dupenloup).

3. As to independent claim 1,

a method of designing a semiconductor integrated circuit [Col. 1, lines 11-16; i.e., a method for designing IC's by utilizing an automated synthesis], comprising:

a first step for determining a number of clocks different in delay amount [Col. 11, lines 1-5 and 49-52; i.e., a plurality of clocks each different in delay are identified.],

which are used for verification of a circuit design of the semiconductor integrated circuit upon the circuit design thereof [Col. 12, lines 27-39; i.e., identified clocks are utilized in the verification of the circuit design.], and

determining delays in the clocks on the basis of pre-set conditions for constraints of timings [Col. 17, lines 12-13, Col. 41, lines 34-45, Col. 52, lines 63-65,

and Col. 53, lines 10-15; i.e., constraints, timing budgets, and clock definitions each provide delay values for clocks on the basis of design rules/constraints/directives (see Fig. 19: element 454).];

a second step for allocating clocks supplied to respective circuits [Col. 54, lines 66-67 to Col. 55, lines 1-2; i.e., clocks are defined on clock nets using a compiler's "create_clock" command in an initial/generic netlist (see Fig. 12: element 358 or Fig. 36: element 333).]; and

a third step for optimizing timings on the basis of a list obtained by the timing constraint conditions and the clock allocation [Col. 42, lines 10-19 and Fig. 36: element 334; i.e., the initial/generic netlist is optimized by the timing constraints (i.e., Dupenloup's constraints, timing budgets, and clock definitions) and initially defined clocks],

and determining whether results of analyses of the respective timings correspond to violation of the constraints of timings [Col. 2, line 17 and Col. 42, line 10; i.e., verification of the netlist is made with respect to timing constraints and violations are identified.],

wherein the optimization of the timings is repeated according to the constraint violation of the constraints of timings [Col. 42, lines 20-21; i.e., optimization is iteratively performed until timing violations are solved];

and the first, second, and third steps are performed prior to performing a layout design of the semiconductor integrated circuit [Col. 79, lines 56-67; i.e., Dupenloup's teachings relating to the first, second, and third steps are directed to circuit/logic design and result in a netlist (see Fig. 1: element 110, Fig. 19: element 456, or Fig. 36: element 337) and layout design is performed after generation of the netlist (see Fig. 1: element 112).].

4. As to Claim 3, a method according to claim 1, further comprising a step for adjusting the delay of each of the clocks again according to the constraint violation when the constraint violation exists in the third step [Col. 13, lines 5-8].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claims 2 and 4-5 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Duplicloup in view of US Patent No. 6,701,506 to Srinivasan et al. (Hereinafter: Srinivasan).

7. Pursuant to claim 2, Duplicloup teaches all of the limitations of claim 1 from which claim 2 depends, including teachings directed to a layout design process. Specifically, Duplicloup teaches the verified and final netlist is an input to start a layout design process yielding a layout design [Col. 80, lines 66-67 and Fig. 1: element 110 (netlist) and element 112 (layout design).]. Furthermore, Duplicloup teaches during layout design process clock trees are generated to distribute clock signals [Col. 11, lines 18-20; i.e., clock trees comprise clocks different in delay as required by the fourth step of claim 2], and teaches “timing closure flows” are used to ensure these clock signals meet timing constraints in layout design [Col. 49, lines 50-58].

8. However, **Duplicloup does not** teach the specific steps involved in “timing closure flows” and therefore does not teach, as required by claim 2, a fifth step for adjusting skews for each of said clocks; a sixth step for adjusting delays respectively

included in the clocks to the determined clock delays upon the layout design; and a seventh step for making an adjustment to a layout that satisfies the timing constraint conditions upon the layout design and determining whether analytical results of the respective timings correspond to the constraint violation, wherein the layout adjustment is repeated according to the constraint violation.

9. **Srinivasan teaches:**

a step for generating clocks different in the delay amount for the verification of a layout design [Fig. 5: element 246; i.e., a generated clock tree comprises clocks different in the delay amount (e.g., see Fig. 6, 7, or 11), and the clock tree is utilized in subsequent verification (Fig. 1: element 115).],

a step for adjusting skews for each of the clocks [Fig. 5: element 248; i.e., skews for the clocks are analyzed and corrected.],

a step for adjusting delays respectively included in the clocks to the determined clock delays upon the layout design [Fig. 5: element 250; i.e., clock delays are adjusted upon layout design (i.e., the layout process starts at element 105 of Fig. 1, and the delays for the clock tree in the layout design are adjusted in element 110 of Fig. 1).], and

a step for making an adjustment to a layout that satisfies timing constraint conditions upon the layout design [Col. 1, lines 63-67 to Col. 2, lines 1-4; i.e., a physical optimization step is provided to recursively ensure the placement of the layout meets timing constraints by performing corrections and further optimizations.] and
determining whether analytical results of the respective timings correspond to the constraint violation [Col. 1, lines 63-67 to Col. 2, lines 1-4; i.e., timing analysis is performed to detect timing violations.],

wherein the layout adjustment is repeated according to the constraint violation [Col. 1, lines 63-67 to Col. 2, lines 1-4; i.e., the physical optimization step recursively performs corrections on timing violations.].

10. **It would have been obvious** to one of ordinary skill in the art at the time of Applicant's invention to have combined the teachings of Dupenloup with Srinivasan to provide the above steps involved in performing the layout design's timing closure contemplated by Dupenloup [Dupenloup: Col. 49, lines 50-58], since such steps ensure the design and timing constraints of the physical/layout design comply with the design and timing constraints of the circuit/logic design [Srinivasan: Col. 1, lines 32-35] and such steps are part of the typical design flow [Srinivasan: Col. 1, line 27].

11. Pursuant to claim 4, a method according to claim 2, further comprising a step for adjusting delays set for said clocks according to the constraint violation when the constraint violation occurs in the seventh step [Srinivasan: Col. 2, lines 1-2].

12. Pursuant to claim 5, a method according to claim 4, wherein adjusting the delays comprises adding an delay at a starting point where data is outputted [Srinivasan: Col. 2, lines 1-2; Fig. 18: element 454], and determining the clock delays according to the difference between the added value and the cycle of the clock [Srinivasan: Col. 19, lines 10-19; Fig. 18: elements 456 and 458].

Response to Arguments

13. Applicant's arguments contained the Appeal Brief have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Suresh Memula whose telephone number is (571) 272-8046, and any inquiry for a formal Applicant initiated interview must be requested via a PTOL-413A form and faxed to the Examiner's personal fax phone number: (571) 273-8046. Furthermore, Applicant is invited to contact the Examiner via email (suresh.memula@uspto.gov) on the condition the communication is pursuant to and in accordance with MPEP §502.03 and §713.01. The Examiner can normally be reached Monday-Thursday 8am-6:30pm EST. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned (i.e., central fax phone number) is 571-273-8300.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Suresh Memula/
Examiner, Art Unit 2825
April 14, 2010

/Jack Chiang/

Supervisory Patent Examiner, Art Unit 2825